ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit test method which reduces the required data volume for testing and efficiently detects faults in a circuit to be tested, the method comprising means 110 to generate identical pattern sequences repeatedly and means 120 to control flipped bits in pattern sequences, in order to generate neighborhood pattern sequences and use the neighborhood patterns to test the circuit under test 130. The neighborhood patterns include, in whole or in part, such pattern sequences as ones without flipped bits, ones with all or some flipped bits in one pattern and ones with all or some flipped bits in consecutive patterns or patterns at regular intervals, the interval being equivalent to a given number of patterns. Because a test pattern generator is provided independently of the circuit to be tested, the problem of a prolonged design period can be eliminated, a loss in the operating speed of the circuit under test is minimized and a high fault coverage can be achieved with less hardware overhead and a smaller volume of test data.